Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1-2. (canceled)

3. (currently amended) A cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously providing a first gas including an etching agent having an etching action with respect to the semiconductor layer and a second gas including a crystal growth source material to the surface of the semiconductor layer, wherein the first gas and the second gas are supplied in an intermittent manner,

wherein an absolute value for a rate of change in thickness of the semiconductor layer during the cleaning treatment step is 0.1 nm/sec or less,

wherein a symbol for the rate of change of the layer thickness of the semiconductor layer is positive when the layer thickness increases and is negative when layer thickness decreases;

the rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R;

a rate of change of layer thickness of the semiconductor layer when only supplying the first gas to the semiconductor layer surface is r_1;

a rate of change of layer thickness of the semiconductor layer when only supplying the second gas to the semiconductor layer surface is r_2; and

the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes:

$$|R| < |r_2| < |r_1|.$$

4. (previously presented) The cleaning treatment method according to claim 3, wherein the first gas and the second gas are supplied intermittently for fixed periods of time, where a time of supplying the first and second gases and a time of not supplying the first and second gases are alternately repeated.

5. (previously presented) The cleaning treatment method according to claim 3, wherein a difference in layer thickness of the semiconductor layer before and after implementation of the cleaning treatment step is 100 nm or less.

6. (previously presented) The cleaning treatment method according to claim 3, wherein layer thickness of the semiconductor layer is not substantially reduced during implementation of the cleaning treatment step.

7. (previously presented) The cleaning treatment method according to claim 5, wherein the rate of change in layer thickness of the semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material.

8. (canceled)

9. (currently amended) The cleaning treatment method according to claim [[8]]3, wherein $R < 0$.

10. (canceled)

11. (previously presented) The cleaning treatment method according to claim 3, wherein the crystal growth source material includes an element constituting the semiconductor layer.

12. (previously presented) The cleaning treatment method according to claim 3, wherein the crystal growth source material includes organic metal.

13. (previously presented) The cleaning treatment method according to claim 3, wherein the etching agent is a halogen element or compound thereof.

14. (previously presented) The cleaning treatment method according to claim 3, wherein the semiconductor layer is comprised of compound semiconductor.

15. (original) The cleaning treatment method according to claim 14, wherein the semiconductor layer is comprised of a group III - V compound semiconductor.

16. (original) The cleaning treatment method according to claim 15, wherein the crystal growth source material is a compound including a group III element constituting the semiconductor layer.

17. (previously presented) The cleaning treatment method according to claim 15, wherein the group III element constituting the semiconductor layer is comprised of a single species.

18. (previously presented) The cleaning treatment method according to claim 15, wherein the group III element constituting the semiconductor layer is indium (In).

19-20. (canceled)

21. (currently amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer at an upper part of a semiconductor substrate;

subjecting the surface of the first semiconductor layer to cleaning treatment; and

forming a second semiconductor layer on the first semiconductor layer,

wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of simultaneously supplying a first gas including an etching agent having an etching action with respect to the semiconductor layer and a second gas including a crystal growth source material to

the surface of the semiconductor layer, where the first gas and the second gas are supplied in an intermittent manner, and

an absolute value for a rate in thickness of the first semiconductor layer during the cleaning treatment step is 0.1 nm/sec or less,

wherein when it is taken that:

a symbol for rate of change of layer thickness of the first semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases;

the rate of change of layer thickness of the first semiconductor layer during implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment is R;

a rate of change of layer thickness of the first semiconductor layer in the case of supplying only the first gas to the first semiconductor layer surface is r_1, and

a rate of change of layer thickness of the first semiconductor layer in the case of supplying only the second gas to the first semiconductor layer surface is r_2,

the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes:

$$|R| < |r_2| < |r_1|.$$

22. (previously presented) The method of manufacturing a semiconductor device according to claim 21, wherein the first gas and the second gas are supplied intermittently for fixed periods of time, where a time of supplying the first and second gases and a time of not supplying the first and second gases are alternately repeated.

23. (previously presented) The method of manufacturing a semiconductor device according to claim 21, wherein a difference in the layer thickness of the first semiconductor layer before and after implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment is 100 nm or less.

24. (previously presented) The method of manufacturing a semiconductor device according to claim 21, wherein the layer thickness of the first semiconductor layer is not substantially reduced during implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment.

25. (previously presented) The method of manufacturing a semiconductor device according to claim 23, wherein the rate of change in the layer thickness of the first semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material.

26. (canceled)

27. (currently amended) The method of manufacturing a semiconductor device according to claim [[26]]21, wherein $R < 0$.

28. (canceled)

29. (previously presented) The method of manufacturing a semiconductor device according to claim 21, wherein the crystal growth source material includes an element constituting the first semiconductor layer.

30. (previously presented) The method of manufacturing a semiconductor device according to claim 21, wherein the crystal growth source material includes a metal organic.

31. (previously presented) The method of manufacturing a semiconductor device according to claim 21, wherein the etching agent is a halogen element or compound thereof.

32. (previously presented) The method of manufacturing a semiconductor device according to claim 21, wherein the first semiconductor layer is comprised of compound semiconductor.

33. (original) The method of manufacturing a semiconductor device according to claim 32, wherein the first semiconductor layer is comprised of compound semiconductor.

34. (original) The method of manufacturing a semiconductor device according to claim 33, wherein the crystal growth source material includes a group III element constituting the first semiconductor layer.

35. (original) The method of manufacturing a semiconductor device according to claim 34, wherein the group III element constituting the semiconductor layer is a single species.

36. (original) The method of manufacturing a semiconductor device according to claim 35, wherein the group III element constituting the semiconductor layer is indium (In).

37. (previously presented) The method of manufacturing a semiconductor device according to claim 21, wherein the first semiconductor layer and the second semiconductor layer are formed using vapor phase epitaxy.

38. (previously presented) The method of manufacturing a semiconductor device according to claim 21, wherein a mask is formed on the first semiconductor layer after the step of forming the first semiconductor layer, and after eliminating the mask, the step of subjecting the surface of the first semiconductor layer to cleaning treatment is implemented.

39-48. (canceled)

49. (previously presented) A cleaning treatment method according to claim 3, wherein a concentration of residual Si of said surface of said semiconductor layer is a surface density of 5×10^{11} atoms/cm^2 or less.

50. (previously presented) A cleaning treatment method according to claim 3, wherein a concentration of residual Si of said surface of said semiconductor layer is a surface density of 2.5×10^{11} atoms/cm^2 or less.

51. (previously presented) A method of manufacturing a semiconductor device according to claim 21, wherein a concentration of residual Si of a regrowth interface of the

semiconductor layer is a surface density of 5 x 10^{11} atoms/cm^2 or less.

52. (currently amended) A ~~cleaning treatment~~ method of manufacturing a semiconductor device according to claim 21, wherein a concentration of residual Si of a regrowth interface of the semiconductor layer is a surface density of 2.5 x 10^{11} atoms/cm^2 or less.

53. (previously presented) A cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously providing a first gas including an etching agent having an etching action with respect to the semiconductor layer and a second gas including crystal growth source material to the surface of the semiconductor layer,

wherein when it is taken that: a symbol for rate of change of layer thickness of the semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases;

the rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R;

a rate of change of layer thickness of the semiconductor layer in the case of supplying only the first gas to the semiconductor layer surface is r_1;

a rate of change of layer thickness of the semiconductor layer in the case of supplying only the second gas to the semiconductor layer surface is r_2; and

the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes:

$$|R| < |r_2| < |r_1|.$$

54. (previously presented) The cleaning treatment method according to claim 53, wherein $|R|$ is 0.1 nm/sec or less.

55. (previously presented) The cleaning treatment method according to claim 53, wherein a difference in layer thickness of the semiconductor layer before and after implementation of the cleaning treatment step is 100 nm or less.

56. (previously presented) A cleaning treatment method according to claim 53, wherein a concentration of residual Si of said surface of said semiconductor layer is a surface density of 5×10^{11} atoms/cm^2 or less.

57. (previously presented) A cleaning treatment method according to claim 53, wherein a concentration of residual Si of said surface of said semiconductor layer is a surface density of 2.5×10^{11} atoms/cm^2 or less.